

JO11 Rec'd PCT/PTO 15 MAR 2001

FORM PTO-1390 (REV 11-98)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER  5000.113
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known see 37 CFR 1.5) <b>09/787189</b>
INTERNATIONAL APPLICATION NO. PCT/US99/21475	INTERNATIONAL FILING DATE September 16, 1999	PRIORITY DATE CLAIMED September 16, 1998	
TITLE OF INVENTION LOW TEMPERATURE FORMATION OF BACKSIDE OHMIC CONTACTS FOR VERTICAL DEVICES			
APPLICANT(S) FOR DO/EO/US David B. SLATER, Jr.			

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
  - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☐ has been transmitted by the International Bureau.
  - c. ☒ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
  - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☐ have been transmitted by the International Bureau.
  - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
  - d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

**Items 11. to 16. below concern document(s) or information included:**

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.  
☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

Certificate of Mailing Under 37 CFR 1.10

Express Mail Label No. EL616946359US

March 15, 2001

I hereby certify that this correspondence is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box PCT, Assistant Commissioner for Patents, Washington, DC 20231.

Philip Summa

U.S. APPLICATION NO. (if known, see 37 CFR 1.53) <div style="font-size: 2em; font-weight: bold;">097787189</div>		INTERNATIONAL APPLICATION NO. PCT/US99/21475		ATTORNEY'S DOCKET NUMBER 5000.113	
---	--	---	--	--------------------------------------	--

17. <input checked="" type="checkbox"/> The following fees are submitted: <b>BASIC NATIONAL FEE ( 37 CFR 1.492 (a) (1) - (5) ) .</b> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO ----- \$1000.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ----- \$860.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ----- \$710.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) ----- \$690.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) ----- \$100.00 <div style="text-align: right;"><b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b></div>	<b>CALCULATIONS</b> PTO USE ONLY																									
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	\$ 860.00																									
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <th style="width:20%;">CLAIMS</th> <th style="width:20%;">NUMBER FILED</th> <th style="width:20%;">NUMBER EXTRA</th> <th style="width:20%;">RATE</th> <th style="width:20%;"></th> <th style="width:20%;"></th> </tr> <tr> <td>Total claims</td> <td>20    -20 =</td> <td>0</td> <td>X \$18.00</td> <td>\$ -0-</td> <td>0</td> </tr> <tr> <td>Independent claims</td> <td>3        -3 =</td> <td>0</td> <td>X \$80.00</td> <td>\$ -0-</td> <td>0</td> </tr> <tr> <td colspan="3">MULTIPLE DEPENDENT CLAIM(S) (if applicable)</td> <td>+ \$270.00</td> <td>\$ -0-</td> <td></td> </tr> </table>	CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE			Total claims	20    -20 =	0	X \$18.00	\$ -0-	0	Independent claims	3        -3 =	0	X \$80.00	\$ -0-	0	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$270.00	\$ -0-			
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE																							
Total claims	20    -20 =	0	X \$18.00	\$ -0-	0																					
Independent claims	3        -3 =	0	X \$80.00	\$ -0-	0																					
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$270.00	\$ -0-																						
<b>TOTAL OF ABOVE CALCULATIONS =</b>			\$ 860.00																							
Reduction of 1/2 for filing by small entity, if applicable. A Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).			\$																							
<b>SUBTOTAL =</b>			\$																							
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			\$ -0-																							
<b>TOTAL NATIONAL FEE =</b>			\$ 860.00																							
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property			\$ -0-																							
<b>TOTAL FEES ENCLOSED =</b>			\$ 860.00																							

	<b>Amount to be:</b> <b>refunded</b>	\$
	<b>charged</b>	\$

a. ☒ A check in the amount of \$ 860.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \$ \_\_\_\_\_ to cover the above fees.  
 A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any  
 overpayment to Deposit Account No. 50-0332. A duplicate copy of this sheet is enclosed.

**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.**

SEND ALL CORRESPONDENCE TO

**PHILIP SUMMA, P.A.**  
**13777 Ballantyne Corporate Place**  
**Suite 315**  
**Charlotte, NC 28277**  
**Phone: 704-945-6700**  
**Fax: 704-945-6735**

SIGNATURE.  
 Philip Summa - March 15, 2001  
 NAME  
 31,573  
 REGISTRATION NUMBER

LOW TEMPERATURE FORMATION OF BACKSIDE OHMIC  
CONTACTS FOR VERTICAL DEVICES

FIELD OF THE INVENTION

5 The present invention relates to ohmic contacts to semiconductor materials. In particular, the invention relates to methods of forming ohmic contacts to devices that include a plurality of semiconductor materials.

BACKGROUND OF THE INVENTION

10 In the microelectronics context, circuits are made from the sequential connection of semiconductor devices. Generally speaking, semiconductor devices are operated by, and are used to control, the flow of electric current within specific circuits to accomplish particular tasks. To connect semiconductor devices to one another, appropriate contacts must be made between the semiconductor devices. Because of their high conductivity, the most useful and convenient materials for  
15 carrying current from one device to another are metals.

Such metal contacts should interfere either minimally or preferably not at all with the operation of the device or the current carrying metal. Furthermore, the metal contact must be physically and chemically compatible with the semiconductor material to which it is attached. The types of contact that exhibit these desired  
20 characteristics are known as "ohmic contacts".

An ohmic contact is usually defined as a metal-semiconductor contact that has a negligible contact resistance relative to the bulk or spreading resistance of the semiconductor, Sze, Physics of Semiconductor Devices, Second Edition, 1981, page 304. As further stated therein, an appropriate ohmic contact will not significantly  
25 change the performance of the device to which it is attached, and it can supply any required current with a voltage drop that is appropriately small compared with the drop across the active region of the device.

Ohmic contacts and methods of producing ohmic contacts are known in the art. For example, U.S. Patents 5,409,859 and 5,323,022 to Glass et al. ("Glass  
30 patents"), discuss an ohmic contact structure formed of platinum and p-type silicon carbide and a method of making the ohmic structures. L. Spieß et al., "Aluminium Implantation of p-SiC for Ohmic Contacts," Diamond and Related Materials, vol. 6, pp. 1414-1419 (1997); J. Chen et al., "Contact Resistivity of Re, Pt and Ta Films On

n-type  $\beta$ -SiC: preliminary results," Materials and Science Engineering, B29, pp. 185-189 (1995); and WO 98/37584 also discuss ohmic contacts and SiC.

Although ohmic contacts and methods of making them are known, the known methods for producing ohmic contacts, and especially

those produced using a silicon carbide substrate, are difficult even when properly conducted.

The problems associated with obtaining ohmic contacts are myriad and cumulative. Limited electrical conductivity of the semiconductor due to low hole or electron concentrations may hinder or even prevent the formation of an ohmic contact. Likewise, poor hole or electron mobility within the semiconductor may hinder or even prevent the formation of an ohmic contact. As discussed in the Glass patents, work function differences between the contact metal and semiconductor may give rise to a potential barrier resulting in a contact exhibiting rectifying (non-ohmic) current flow versus applied voltage. Even between two identical semiconductor materials in intimate contact with greatly differing electron-hole concentrations, a potential barrier (built-in potential) may exist, leading to a rectifying rather than ohmic contact. In the Glass patents, these problems were addressed by inserting a distinct p-type doped SiC layer between the p-type SiC substrate and the contact metal.

More difficult problems are encountered when forming ohmic contacts for newer generation gallium and indium based semiconductor devices. The formation of an ohmic contact between a semiconductor and a metal requires the correct alloying of the semiconductor and the contact metal at their interface. Selectively increasing the hole/electron concentration at the semiconductor surface where the ohmic contact metal is deposited is known as an effective means for enhancing the contact process to achieve an ohmic contact. This process is typically achieved through ion implantation, which is well recognized as a selective doping technique in silicon and silicon carbide technologies. However, in the case of silicon carbide, ion implantation is usually performed at elevated temperatures (typically  $>600^{\circ}\text{C}$ ) in order to minimize damage to the silicon carbide crystal lattice. "Activating" the implanted atoms to achieve the desired high carrier concentrations often requires anneal temperatures in excess of  $1600^{\circ}\text{C}$ , often in a silicon over pressure. The equipment required for this ion implantation technique is specialized and expensive.

After the high temperature ion implant and subsequent anneal, the contact metal is deposited on the implanted substrate surface and annealed at temperatures in excess of  $900^{\circ}\text{C}$ . This method of forming contacts on semiconductor devices that

incorporate gallium nitride or indium gallium nitride is not feasible because these compounds disassociate at elevated temperatures.

One theoretical answer to this problem would be to form an ohmic contact on the substrate prior to growing the delicate epitaxial layers (e.g. gallium nitride layers) necessary to complete the semiconductor device. This approach is undesirable, however, because it inserts an undesired contaminant, the contact metal, into the epitaxial growth system. The contaminant metal can effect epitaxial growth by interfering with lattice growth, doping, rate of reaction or all of these factors. In addition, metal impurities can degrade the optical and electrical properties of the epitaxial layers.

Similarly, many semiconductor devices such as metal-oxide-semiconductor field-effect transistors ("MOSFETS") require a layer of a semiconductor oxide (e.g. silicon dioxide). The high temperatures associated with traditional ion implantation techniques and implant or contact metal annealing processes place high stress on oxide layers, which can damage oxide layers, the semiconductor-oxide interface and the device itself. Alternatively, forming the ohmic contact prior to creating the oxide layer is not practical because the oxidizing environment utilized to form the oxide layers has adverse effects on the ohmic contact.

Accordingly, a need exists for a practical and economical method for forming an ohmic contact for use in conjunction with a semiconductor device that does not exhibit the manufacturing problems previously discussed. The need also exists for a type of a semiconductor device that incorporates an ohmic contact but is economic to manufacture.

#### OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention is to provide a semiconductor device that incorporates an ohmic contact.

It is a further object of the invention to provide a semiconductor device comprising silicon carbide and an ohmic contact.

It is a further object of the invention to provide a semiconductor device that incorporates an ohmic contact that is economic to manufacture.

It is a further object of the invention to provide a method for forming a

semiconductor device that incorporates an ohmic contact.

The invention meets these objects with a method for forming a metal-semiconductor ohmic contact for a semiconductor device. The method comprises implanting a selected dopant material into a surface of a semiconductor substrate having an initial conductivity type. The implanted dopant provides the same conductivity type as the semiconductor substrate. The dopant implantation is followed by annealing the implanted semiconductor substrate a first time at a temperature and for a time sufficient to activate the implanted dopant atoms and increase the effective carrier concentrations. Depositing a metal on the implanted surface of the semiconductor material follows the first anneal. Thereafter, an annealing of the metal and the implanted semiconductor material occurs. This second anneal is at a temperature below which significant degradation of any epitaxial layers placed on the substrate would occur, but high enough to form an ohmic contact between the implanted semiconductor material and the deposited metal.

The invention also meets these objects with a semiconductor device comprising a semiconductor substrate having a first surface and a second surface and a first conductivity type. The device also comprises at least one epitaxial layer that is grown or placed upon the first surface of the semiconductor substrate. The semiconductor substrate is further defined as having a zone of increased carrier concentration in the substrate extending from the second surface (the surface opposite the epitaxial layer) toward the first surface. The device further comprises a layer of metal deposited on the second surface of the substrate to form an ohmic contact at the interface of the metal and the zone of increased carrier concentration.

The foregoing and other objects, advantages and features of the invention and the manner in which the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings, which illustrate exemplary embodiments, and wherein:

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic cross-sectional diagram of a semiconductor device according to the present invention.

FIG. 2 is a schematic cross-sectional diagram of a dopant implantation as utilized in the method according to the invention.

#### DETAILED DESCRIPTION

The present invention is a semiconductor device incorporating an ohmic  
5 contact and a method of forming the ohmic contact.

It will be understood by those familiar with wide bandgap semiconductors, such as silicon carbide, and semiconductor devices formed therefrom that the invention is most useful in making a semiconductor device and ohmic contact utilizing n-type or p-type silicon carbide ("SiC"). Accordingly, for ease of  
10 explanation, the following description of the invention and examples will be directed toward an embodiment of the invention utilizing SiC. Those skilled in the art, however, will readily recognize that the invention may be easily adapted for use with other semiconductor materials such as silicon, gallium nitride, aluminum gallium nitride, and indium gallium nitride. As used herein, aluminum gallium nitride and  
15 indium gallium nitride include compounds where the mole percents of aluminum and gallium or indium and gallium equal 1.

In a broad aspect the invention is a semiconductor device comprising a semiconductor substrate having an initial concentration of dopant imparting an initial conductivity type. The semiconductor substrate may be either n-type or p-type. The  
20 device also comprises at least one epitaxial layer situated adjacent one surface of the semiconductor substrate.

The claimed semiconductor device is further characterized in that the semiconductor substrate is defined by a zone of increased carrier concentration extending from the surface of the substrate opposite the epitaxial layers toward the  
25 surface adjacent the epitaxial layers. A layer of metal is deposited on the substrate at the zone of increased carrier concentration to form an ohmic contact at the interface of the metal and the substrate.

Referring now to FIG. 1, a schematic of a semiconductor device 10 according to the invention is presented. The device 10 comprises a semiconductor substrate 12,  
30 which for purposes of explanation is considered to be SiC. It should be understood, however, that other semiconductor materials, such as silicon, may be used as a

substrate in the practice of the invention. The SiC substrate 12 may be either p-type or n-type.

Situated adjacent the SiC substrate 12 are the additional components 14 necessary to complete the semiconductor device. For example and as represented in FIG. 1, the semiconductor device may be a light emitting diode ("LED") having sequential epitaxial layers 14a, 14b, and 14c of p-type and n-type semiconductor materials. In a preferred embodiment, the invention is a vertical semiconductor device such as a LED, metal-oxide-semiconductor field-effect transistor ("MOSFET"), lasers, or Schottky rectifiers that are comprised of several epitaxial layers situated adjacent a semiconductor substrate. As will be discussed later, the device according to the invention is particularly suited for vertical semiconductor devices that comprise materials having low melting or low disassociation temperatures. Such materials would include gallium nitride, indium gallium nitride and aluminum gallium nitride.

The claimed device is further characterized as having a zone of increased carrier concentration 16 on the backside of the semiconductor substrate. In other words, the semiconductor substrate, in this case SiC, has a carrier concentration near the surface of the substrate opposite the epitaxial layers that is higher than the carrier concentration exhibited in the remainder of the substrate.

The line that serves as the boundary to the zone of increased carrier concentration 16 is dotted to represent the fact that there is no sharp boundary at which the carrier concentration when the substrate 12 suddenly changes. The carrier concentration decreases as the distance from the backside surface of the substrate increases until the carrier concentration equals the initial carrier concentration. As will be discussed below, the zone of increased carrier concentration is formed by a room temperature ion implantation technique using dopants commonly associated with p-type and n-type semiconductor materials.

For example and still referring to FIG. 1, a preferred embodiment of the claimed device comprises a n-type SiC substrate doped with nitrogen. It should be understood that n-type SiC formed of other n-type dopants along with the various types of p-type SiC also may be used in accordance with the invention. The SiC

substrate 12 is preferably slightly to highly doped and possess an initial carrier concentration between about  $1 \times 10^{15}$  and about  $1 \times 10^{19} \text{ cm}^{-3}$ . The terms "slightly" and "highly" are imprecise and are purposely used to show that the initial carrier concentration may vary considerably. Although the initial carrier concentration may vary considerably, testing has shown that substrates that are initially moderate to highly doped provide the best results. Through ion implantation of a selected dopant material (e.g. nitrogen) at the surface opposite the epitaxial layers 14, a zone 16 is created that contains a higher carrier concentration than the remainder of the substrate 12. Preferably, the ion implantation is conducted at a level that creates a zone of increased carrier concentration 16 on the backside of the substrate that exhibits a carrier concentration between about  $1 \times 10^{18}$  and about  $1 \times 10^{20} \text{ cm}^{-3}$  and that is always higher than the initial carrier concentration.

Those skilled in the art will recognize that a zone of increased carrier concentration as described previously may also be formed during the growth of the substrate. However, the difficulties associated with the variable feed rates of the required dopants and other difficulties typically associated with crystal growth methods make this approach impractical.

The preferred n-type dopants for use in forming the zone of increased carrier concentration 16 are nitrogen, arsenic and phosphorous. Preferred p-type dopants for use in forming the zone of increased carrier concentration 16 are aluminum, boron and gallium.

Although Applicant does not wish to be bound by a particular theory, evidence suggests that the zone of increased carrier concentration 16 allows for the creation of a metal contact that exhibits ohmic properties. In a preferred embodiment, a selected contact metal 18 having a melting point, vapor pressure and physical and chemical properties suitable for use with the overall semiconductor device is deposited at the surface of the SiC substrate at the zone of increased carrier concentration 16 to form an interface 20 between the metal and the substrate. Preferred metals include nickel, palladium, platinum, aluminum and titanium with nickel being most preferred. The device, including the metal and the substrate is then annealed at a temperature low

enough to avoid damage to the device and specifically any epitaxial layer, but high enough to form an ohmic contact at the interface of the metal and substrate.

Again, although the Applicant does not wish to be bound by any particular theory, it appears useful to create the zone of increased carrier concentration to serve as the receptor for the contact metal. Thus, in another embodiment, the invention  
5 comprises the method of forming the ohmic contact utilized in the previously described semiconductor device.

In a broad aspect, the invention is a method for forming a metal-semiconductor contact for a semiconductor device. The method comprises implanting  
10 a selected dopant material into a semiconductor substrate having a first conductivity type and wherein the implanted dopant provides the same conductivity type as the substrate. For purposes of this discussion it will be assumed that the semiconductor substrate is a SiC substrate and that the dopant material is deposited into a surface of the SiC substrate. Those skilled in the art, however, will readily recognize that the  
15 invention may be easily adapted for use with other semiconductor materials. An annealing step follows the implanting of the selected dopant material. In this annealing step the implanted SiC substrate is annealed at a temperature and for a time sufficient to activate the implanted dopant atoms to effectively increase the carrier concentration of the implanted dopant atoms in the SiC substrate. A contact metal is  
20 then deposited on the implanted surface of the SiC substrate. The deposited contact metal and the implanted surface of the SiC substrate are then annealed. This second annealing is at a temperature below that at which any expitaxial layer placed on the substrate would experience significant degradation but high enough to form an ohmic contact between the implanted SiC and the deposited metal.

25 In a preferred embodiment, the semiconductor substrate may comprise a n-type or p-type substrate that may possess a slight, moderate, or high initial dopant concentration. For example, where n-type SiC is the substrate, the SiC substrate may possess an initial dopant concentration from about  $1 \times 10^{15}$  (slightly doped) to  $1 \times 10^{19}$   $\text{cm}^{-3}$  (highly doped). The terms "slight," "moderate," and "high" are imprecise and  
30 are used to indicate that the initial concentration of dopant in the substrate material may vary. Testing has shown that moderate to highly doped substrates achieve the

best results with the invention.

The semiconductor substrate is then implanted with a selected dopant material and annealed. Preferably, the dopant implantation occurs at room temperature and the subsequent annealing occurs at a temperature between about 800°C and about 1300°C. Dopants usually associated with the conductivity type of the substrate may be used as the dopant for the implantation step. For example, when n-type SiC initially doped with nitrogen is the substrate, nitrogen may serve as the implanted dopant. Likewise, when p-type SiC initially doped with aluminum is the substrate, aluminum may serve as the implanted dopant. Other possible n-type dopants are arsenic and phosphorous. Boron and gallium may serve as alternative p-type dopants.

Those skilled in the art will readily recognize that the implanting of the dopant material may be accomplished at high temperatures. In fact, high temperature implantation is typically preferred in the SiC context in order to reduce damage to the SiC lattice structure. In the SiC context, however, high temperature ion implantation places constraints on the commercial use of the invention. Ion implanting equipment with the capability of heating the SiC substrate during implantation are atypical, expensive and intended for research and development rather than low cost, high volume applications. Furthermore, when SiC substrates are heated to high temperatures, they must be heated and cooled at a rate that will not produce fractures thereby slowing down the production process.

Accordingly, room temperature implantation is the preferred implantation method for use in the invention. It has been discovered that room temperature implanting of dopant followed by an annealing step in a simple vented furnace capable of reaching 1300°C and holding 100 or more substrate wafers achieves satisfactory results and greatly increases throughput.

The room temperature implantation of dopant is preferably conducted so as to create a zone of increased dopant concentration near the implanted surface of the semiconductor substrate. FIG. 2 is a schematic representation of the implantation process according to the invention. In this example, a n-type SiC substrate **22** having an initial dopant concentration of approximately  $1 \times 10^{18} \text{ cm}^{-3}$  is implanted with atomic or diatomic nitrogen **24** at energies of 10 to 60 keV with doses of  $1 \times 10^{13} \text{ cm}^{-2}$  or more.

In some instances more than one implant energy may be used to create a more graduated carrier concentration distribution. The implantation process produces a zone 26 near the implanted surface of the SiC substrate approximately 1000 angstroms in depth having a total chemical dopant concentration of approximately  
5  $1 \times 10^{19}$  to  $1 \times 10^{20} \text{ cm}^{-3}$  with the concentration of the implanted dopant decreasing as the distance from the implanted surface increases. The dopant concentration outside of the zone of increased dopant concentration 26 remains substantially the same as the initial dopant concentration. The boundary of the zone of increased carrier concentration 26 is represented as a dotted line to indicate that the change in carrier  
10 concentration between the zone 26 and the remainder of the substrate is not distinct but gradual. Those skilled in the art should recognize that the implantation energy or the dose may be readily changed to achieve desired concentrations and thicknesses.

As mentioned previously, it is necessary to anneal the implanted substrate. The annealing is required because some of the implanted dopant ions are not "active"  
15 immediately after implantation. The term "active" is used to describe the availability of the implanted ions to contribute to the overall carrier concentration of the implanted substrate.

During implantation, the crystal lattice of the SiC substrate is essentially bombarded by dopant ions. These ions crash into the crystal lattice where they are  
20 retained. This bombardment does not result in a perfect insertion of dopant ions into the existing crystal lattice. The initial positioning of many of the dopant ions may prevent the ions from being "active" participants in the crystal lattice, which itself may be damaged by the bombardment. Annealing (*i.e.*, heating) the implanted SiC substrate provides a mechanism by which the implanted ions and the crystal lattice of  
25 the substrate may rearrange in a more orderly fashion and recover from the damage incurred during the dopant implantation.

Using round numbers solely for explanatory purposes, the implanting process may be thought of as follows. If 100 nitrogen ions are implanted in an n-type SiC substrate having an initial concentration of x nitrogen atoms, immediately after  
30 implantation the substrate may only exhibit the characteristics associated with a substrate having "x+10" nitrogen ions. However, if the substrate is then annealed and

the implanted ions are allowed to settle into position in the crystal lattice, the substrate may exhibit the characteristics associated with a substrate having "x+90" nitrogen ions. Thus, the annealing step has "activated" approximately 80 of the implanted nitrogen ions.

5           Testing shows that annealing the room temperature implanted SiC substrate at temperatures between approximately 1000°C and 1300°C for about two hours or less will yield satisfactory results. The temperature and time may be easily adjusted to achieve a more complete activation of the implanted dose.

          The semiconductor device comprising the above-discussed implanted substrate  
10           possesses at least one epitaxial layer. The epitaxial layer may be grown by any means known to those skilled in the art. In one preferred embodiment of the invention, the epitaxial layer is deposited prior to the dopant implantation of the substrate. However, the desired epitaxial layer or subsequently fabricated device may be made of or comprised of a material (e.g., gallium nitride or a silicon oxide) incapable of  
15           withstanding the high temperature anneal of the implanted substrate. In this instance, the epitaxial layer may be formed after the dopant implantation.

          After the semiconductor substrate is implanted and a well annealed zone of increased dopant concentration is established, and any epitaxial layers placed on the substrate, the metal selected to form the ohmic contact is applied to the surface of the  
20           substrate at the zone of increased carrier concentration. The metal may be just about any metal typically used in forming electrical contacts that possesses an appropriately high melting point and vapor pressure and does not interact adversely with the substrate material. Preferred metals include nickel, palladium, platinum, titanium and aluminum with nickel being most preferred.

25           Preferably, the contact metal is deposited on the substrate surface to form a layer 300 angstroms thick or more. The deposition is followed by a second anneal. This anneal, however, is not a high temperature long duration anneal. This anneal preferably occurs at a temperature less than about 1000 ° C and most preferably less than about 800°C for 20 minutes or less and most preferably for 5 minutes or less.  
30           These temperatures and time periods are sufficiently low to avoid damaging any epitaxial layers that are on the substrate. The annealing of the contact metal to the

semiconductor substrate results in an ohmic contact at the interface of the metal and substrate.

In a more specific embodiment of the invention, a metal semiconductor according to the invention was created using a n-type SiC substrate which was first  
5 implanted at an energy of 50 keV with a  $3 \times 10^{14} \text{ cm}^{-2}$  dose of atomic nitrogen followed  
a second implantation at 25 keV at  $5 \times 10^{14} \text{ cm}^{-2}$ . The implantation was followed by an  
activation anneal at 1300 °C for 60 to 90 minutes in an argon ambient in a furnace.  
Subsequently, the contact metal, nickel was deposited on the implanted surface at a  
thickness of 2500 Angstroms. The contact anneal was then performed at 800 °C for 2  
10 minutes in argon. The resulting ohmic contact exhibited satisfactory ohmic  
properties.

Those skilled in the art should recognize that it is also possible to conduct the contact anneal in situ with epitaxial growth.

The invention offers a substantial advantage for vertical devices such as  
15 photodetectors, light emitting diodes (LEDs), lasers, power devices such as metal-  
oxide-semiconductor field-effect transistors (MOSFETs), insulated gate bipolar  
transistors (IGBTs), pn junctions and Schottky rectifiers, and microwave devices  
such as SITs (static induction transistors). In the case of detectors, LEDs and lasers,  
epitaxially grown gallium nitride and indium gallium nitride layers are not to be  
20 subjected to anneals at temperatures that would severely damage the layers. In the  
case of indium gallium nitride, time at elevated temperatures becomes more critical as  
the indium composition of the alloy increases. Reducing the backside contact anneal  
temperature also reduces the potential for cracking in or disassociation of indium or  
gallium components in the strained heteroepitaxial films grown on SiC substrates.

25 In the case of power devices where homoepitaxial films of SiC are grown on  
the substrate and thermally grown or thermally regrown (reoxidized or annealed),  
oxides have an integral role in the device performance and a lower anneal temperature  
is an advantage. The backside metal contact can not be subjected to the oxidizing  
ambient that is required to grow the SiC-silicon dioxide interface, therefore, the  
30 backside ohmic contact must be deposited and annealed after the silicon dioxide is  
grown (reoxidized or regrown). Unfortunately, prior art anneal temperatures of about

850 °C or greater are required to subsequently form a contact to the back of the substrate (more typically 900 to 1050 °C) will create defects at the SiC-silicon dioxide interface due to mismatches in the rate of thermal expansion. This is particularly bad for MOSFETs and IGBTs.

5           SiC technology is in its infancy and many proposed devices and material structures are yet to be examined or developed. Further development of this process may lead to anneal temperatures that are even lower, ultimately leading to an ohmic contact between the metal and the semiconductor as deposited (*i.e.*, no anneal).

10           The invention has been described in detail, with reference to certain preferred embodiments, in order to enable the reader to practice the invention without undue experimentation. However, a person having ordinary skill in the art will readily recognize that many of the components and parameters may be varied or modified to a certain extent without departing from the scope and spirit of the invention. Furthermore, titles, headings, or the like are provided to enhance the reader's  
15           comprehension of this document, and should not be read as limiting the scope of the present invention. Accordingly, only the following claims and reasonable extensions and equivalents define the intellectual property rights to the invention.

14

THAT WHICH IS CLAIMED IS:

1. A method for forming an ohmic contact to silicon carbide (12) for a semiconductor device, the method comprising:

5       implanting at room temperature a selected dopant material into a surface of a silicon carbide substrate (12) thereby forming a layer (16) on the silicon carbide substrate having an increased concentration of dopant material;

          annealing the implanted silicon carbide substrate a first time;

          growing at least one epitaxial layer of a compound other than SiC that dissociates below the dissociation temperature at SiC (14) on the silicon carbide  
10       substrate opposite the implanted surface;

          depositing a layer of metal (18) on the implanted surface of the silicon carbide substrate (12); and thereafter

          annealing the metal (18) and the implanted silicon carbide substrate (12, 16) a  
15       second time at a temperature below that at which significant degradation of the compound forming the epitaxial layer (14) would occur, but high enough to form an ohmic contact between the implanted silicon carbide (12, 16) and the deposited metal.

2. A method according to claim 1 wherein the step of growing the epitaxial  
20       layer (14) on the silicon carbide substrate (12) precedes the first annealing of the implanted silicon carbide substrate (12).

3. A method according to claim 1 wherein the step of growing the epitaxial  
25       layer (14) on the silicon carbide substrate (12) follows the first annealing of the implanted silicon carbide substrate (12).

4. A method according to claim 1 wherein the selected dopant material is  
selected from the group consisting of nitrogen, aluminum, arsenic, phosphorous,  
boron and gallium.

30       5. A method according to claim 1 wherein the first annealing the implanted silicon carbide substrate (12, 16) occurs at a temperature above 1000°C to 1300°C.

15

6. A method according to claim 1 wherein the metal (18) is selected from the group comprising nickel, palladium, platinum, aluminum and titanium.

7. A method according to claim 1 wherein the step of annealing the silicon carbide substrate (12) and the deposited metal (18) occurs at a temperature below 850°C.

8. A semiconductor device (10) comprising:  
a semiconductor substrate (12) having a first surface and a second surface and  
a first conductivity type;  
at least one epitaxial layer (14) on said first surface of said semiconductor substrate (12), said epitaxial layer formed of a material with a dissociation temperature below that of the semiconductor substrate;  
a zone (16) of increased carrier concentration in said semiconductor substrate (12) and extending from said second surface of said semiconductor material toward said first surface; and  
a layer of metal (18) deposited on said second surface of said semiconductor substrates (12) that forms an ohmic contact at the interface (20) of said metal and said zone (16) of increased carrier concentration.

20

9. A semiconductor device according to claim 8 wherein the semiconductor substrate (12) is silicon carbide.

10. A semiconductor device according to claim 8 wherein the implanted dopant material is selected from the group consisting of nitrogen, aluminum, arsenic, phosphorous, boron and gallium.

11. A semiconductor device according to claim 9 wherein the initial carrier concentration in the silicon carbide is between  $1 \times 10^{15}$  to  $1 \times 10^{19} \text{ cm}^{-3}$ .

30

12. A semiconductor device according to claim 11 wherein the carrier concentration in the zone of increased carrier concentration (16) is between  $1 \times 10^{18}$

16

and  $1 \times 10^{20} \text{ cm}^{-3}$  and is greater than the initial carrier concentration in the silicon carbide.

13. A semiconductor device according to claim 8 wherein said epitaxial layers (14) are selected from the group consisting of gallium nitride; aluminum gallium nitride; indium gallium nitride; and oxides of silicon, gallium, aluminum and indium.

14. A semiconductor device according to claim 9 wherein said metal (18) is selected from the group comprising nickel, palladium, platinum, aluminum and titanium.

15. A semiconductor device (10) comprising:  
a silicon carbide substrate (12) having a first surface and a second surface and an initial concentration of dopant imparting an initial conductivity type;  
at least one epitaxial layer (14) on said first surface of silicon carbide substrate (12);  
a zone of increased carrier concentration (16) in said silicon carbide substrate (12) and extending from said second surface of said silicon carbide substrate (12) toward said first surface, said zone of dopant material (16) being characterized by a concentration of dopant that progressively decreases from said second surface toward said first surface; and  
a nickel ohmic contact (18) on said second surface of said silicon carbide substrate (12).

16. A semiconductor device according to claim 15 wherein the implanted dopant material is selected from the group consisting of nitrogen, aluminum, arsenic, phosphorous, boron and gallium.

17. A semiconductor device according to claim 15 wherein the initial carrier concentration in the silicon carbide is between  $1 \times 10^{15}$  to  $1 \times 10^{19} \text{ cm}^{-3}$ .

17

18. A semiconductor device according to claim 17 wherein the carrier concentration in the zone of increased carrier concentration is between  $1 \times 10^{18}$  and  $1 \times 10^{20} \text{ cm}^{-3}$  and is greater than the initial carrier concentration in the silicon carbide.

5

19. A semiconductor device according to claim 15 wherein said epitaxial layers (14) are selected from the group consisting of gallium nitride; aluminum gallium nitride; indium gallium nitride; and oxides of silicon, gallium, aluminum and indium.

10

20. A semiconductor device according to claim 15 wherein the semiconductor device is a vertical device.

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau



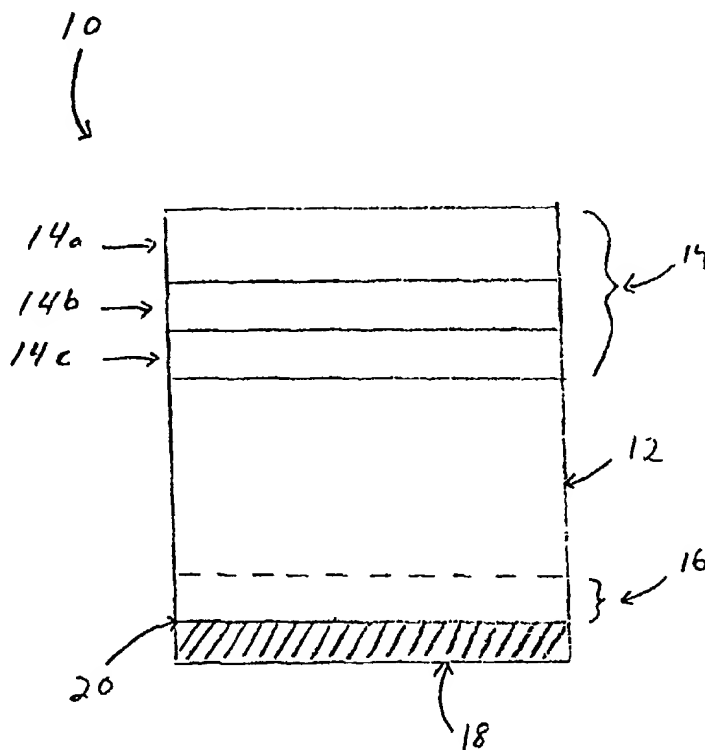
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

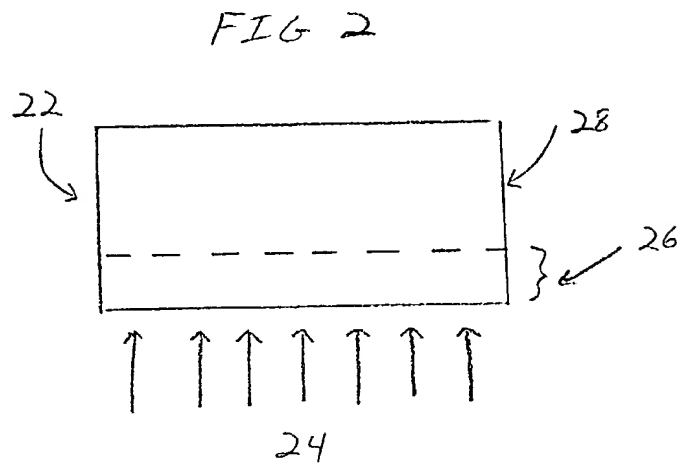
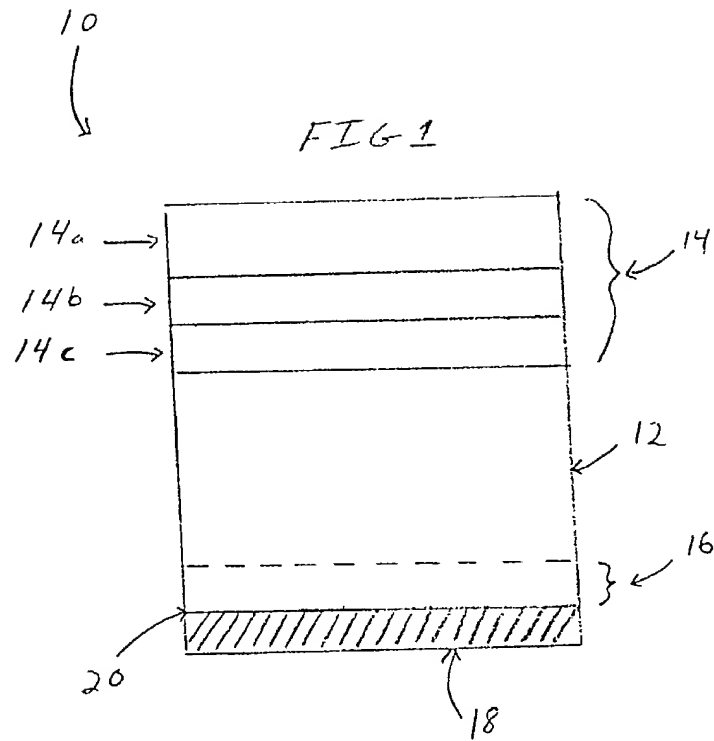
<b>(51) International Patent Classification <sup>7</sup> :</b> <b>H01L 21/04</b>		<b>A1</b>	<b>(11) International Publication Number:</b> <b>WO 00/16382</b>
			<b>(43) International Publication Date:</b> 23 March 2000 (23.03.00)
<b>(21) International Application Number:</b> PCT/US99/21475 <b>(22) International Filing Date:</b> 16 September 1999 (16.09.99) <b>(30) Priority Data:</b> 60/100,546 16 September 1998 (16.09.98) US <b>(71) Applicant (for all designated States except US):</b> CREE RE-SEARCH, INC. [US/US]; 4600 Silicon Drive, Durham, NC 27703-8475 (US). <b>(72) Inventor; and</b> <b>(75) Inventor/Applicant (for US only):</b> SLATER, David, B., Jr. [US/US]; 6304 Jarratt Cove, Raleigh, NC 27613 (US). <b>(74) Agents:</b> SUMMA, Philip et al.; Philip Summa, Patent Attorney, Suite 315, 13777 Ballantyne Corporate Place, Charlotte, NC 28277 (US).			<b>(81) Designated States:</b> AE, AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).  <b>Published</b> <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

**(54) Title:** LOW TEMPERATURE FORMATION OF BACKSIDE OHMIC CONTACTS FOR VERTICAL DEVICES

**(57) Abstract**

The invention comprises a method for forming a metal-semiconductor ohmic contact (18) for use in a semiconductor device (10) having a plurality of epitaxial layers (14a-c) wherein the ohmic contact (18) is preferably formed after deposition of the epitaxial layers (14a-c). The invention also comprises a semiconductor device comprising a plurality of epitaxial layers and an ohmic contact.





Please type a plus sign (+) inside this box



PTO/SB/01 (10-00)

Approved for use through 10/31/2002 OMB 0651-0032

U S Patent and Trademark Office, U S DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

**DECLARATION FOR UTILITY OR  
DESIGN  
PATENT APPLICATION  
(37 CFR 1.63)**

☒ Declaration  
Submitted  
With Initial  
Filing

OR

☐ Declaration  
Submitted after Initial  
Filing (surcharge  
(37 CFR 1.16 (e))  
required)

Attorney Docket Number 5000.113

First Named Inventor David B. Slater, Jr.

**COMPLETE IF KNOWN**

Application Number /

Filing Date

Group Art Unit

Examiner Name

**As a below named inventor, I hereby declare that:**

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**LOW TEMPERATURE FORMATION OF BACKSIDE OHMIC CONTACTS FOR  
VERTICAL DEVICES**

the specification of which (Title of the Invention)

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY)

09/16/1999

as United States Application Number or PCT International

Application Number PCT/US99/21475 and was amended on (MM/DD/YYYY) 09/20/2000 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application

I hereby claim foreign priority benefits under 35 U S C 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below

Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.
60/100,546	09/16/1998	

[Page 1 of 2]

**Burden Hour Statement** This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U S Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

Please type a plus sign (+) inside this box



PTO/SB/01 (10-00)

Approved for use through 10/31/2002. OMB 0651-0032  
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

## DECLARATION — Utility or Design Patent Application

Direct all correspondence to: ☒ Customer Number or Bar Code Label 021176 OR ☐ Correspondence address below

Name	Philip Summa, P.A.		
Address	13777 Ballantyne Corporate Place		
Address	Suite 315		
City	Charlotte	State	NC
ZIP	28277		
Country	Telephone	Fax	
	704-945-6700	704-945-6735	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

NAME OF SOLE OR FIRST INVENTOR:

☐ A petition has been filed for this unsigned inventor

Given Name	David B.	Family Name or Surname	SLATER, Jr.
Inventor's Signature			Date
			3/13/01
Residence: City	State	Country	Citizenship
Raleigh	NC	US	US
Mailing Address 6304 Jarratt Cove			
Mailing Address			
City	State	ZIP	Country
Raleigh	NC	27613	US

NAME OF SECOND INVENTOR:

☐ A petition has been filed for this unsigned inventor

Given Name	Family Name or Surname		
Inventor's Signature	Date		
Residence: City	State	Country	Citizenship
Mailing Address			
Mailing Address			
City	State	ZIP	Country

☐ Additional inventors are being named on the \_\_\_\_\_ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto